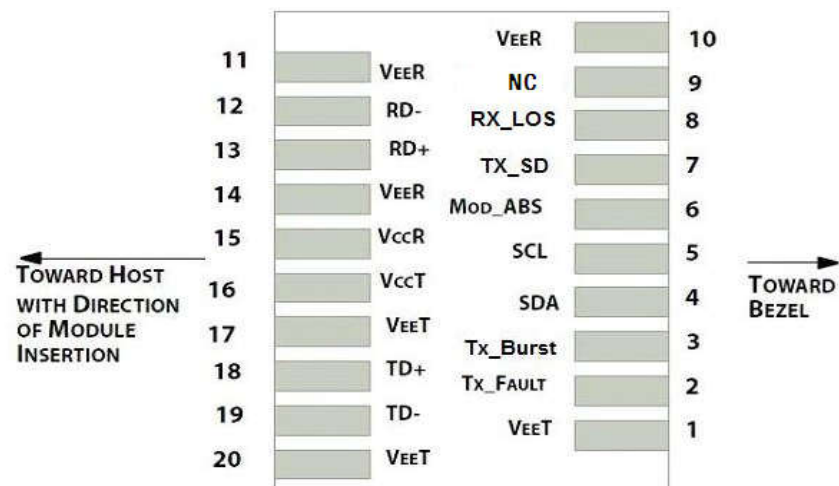


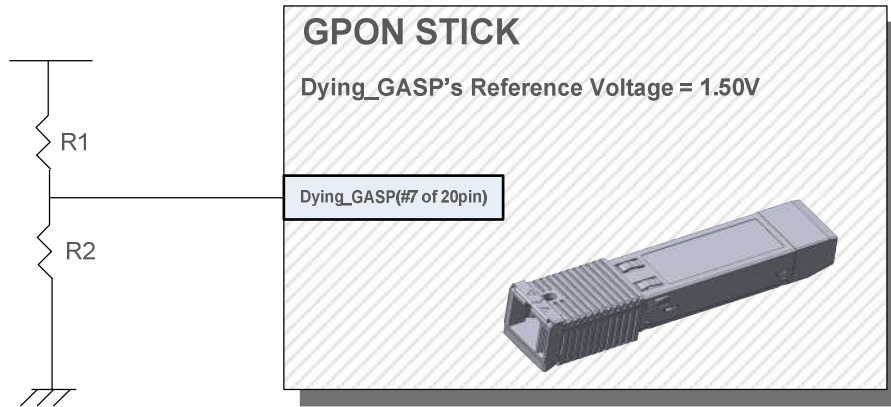
Mean Launched Power (TX Off)	dBm			-45
Extinction Ratio	dB	10		
Optical Return Loss Tolerance	dB	-15		
Transmitter and dispersion Penalty	dB			1
Transmitter Mask (PRBS2 ²³ -1@1.244G)	Compliant With ITU-T G984.2			
Receiver				
Receive Wavelength	nm	1480	1490	1500
Sensitivity (PRBS2 ²³ -1@2.488G, ER=8.2, BER<10 ⁻¹⁰)	dBm			-28
Overload (PRBS2 ²³ -1@2.488G, ER=8.2, BER<10 ⁻¹⁰)	dBm	-8		
Loss of signal De-assert Level	dBm			-29
Loss of signal assert Level	dBm	-39		
LOS Hysteresis	dB	0.5		6
WDM Filter isolation to 1441 nm ~1450 nm, 1530 nm ~1539 nm	dB	25		
WDM Filter isolation to 1250 nm ~1441 nm, 1539 nm~ 1625 nm	dB	36		
Electrical Interface Characteristics				
Data Input Swing Differential/TX	mV	200	-	2000
Data Output Swing Differential/RX	mV	400		1600
Date Differential Impedance	Ω	90	100	110
LVTTL Output High	V	2.4		V _{cc}
LVTTL Output Low	V	0		0.4
LVTTL Input High	V	2.0		V _{cc} +0.3
LVTTL Input Low	V	0		0.8
Timing Characteristics				
Turn On Time at Burst mode (T _{ON})	ns			12.8
Turn Off Time at Burst mode (T _{OFF})	ns			12.8
TX-SD Assert Time (T _{TXSD_ON})	ns			100
TX-SD De-assert Time (T _{TXSD_OFF})	ns			100
LOS Assert Time (T _{LOSA})	us			100
LOS De-assert Time (T _{LOSD})	us			100

PIN Definition

Pin No.	Symbol	Level / Logic	Description
1	VeeT		Module Transmitter Ground
2	Tx_Fault	LVTTTL-O	Module Transmitter Fault
3	Tx_Burst	LVTTTL-I	Transmitter Burst Control, transmitter on when Tx_Burst low
4	SDA	LVTTTL-I	2-Wire Serial Interface Data Line
5	SCL	LVTTTL-I/O	2-Wire Serial Interface Clock
6	MOD_ABS	LVTTTL-O	Module Absent, connected to ground in the module
7	Dying_Gasp	LVTTTL-I	Dying_Gasp Input Reference Voltage Level
8	RX_LOS	LVTTTL-O	Loss of Receiver Signal Indication
9	NC		
10	VeeR		Module Receiver Ground
11	VeeR		Module Receiver Ground
12	RD-	CML-O	Receiver Inverted Data Output, AC-coupled
13	RD+	CML-O	Receiver Non-Inverted Data Output, AC-coupled
14	VeeR		Module Receiver Ground
15	VccR		Module Receiver 3.3V Supply
16	VccT		Module Transmitter 3.3V Supply
17	VeeT		Module Transmitter Ground
18	TD+	LVPECL-I	Transmitter Non-Inverted Data Input, DC-coupled
19	TD-	LVPECL-I	Transmitter Inverted Data Input, DC-coupled
20	VeeT		Module Transmitter Ground



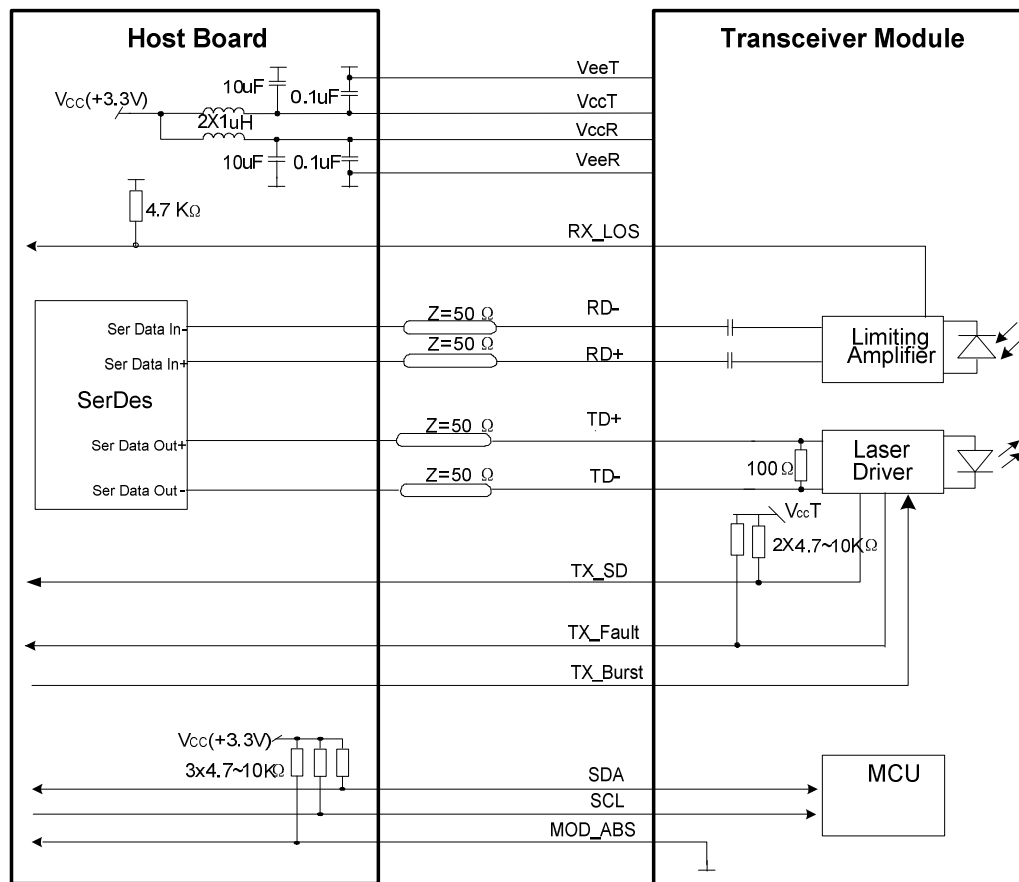
Dying_Gasp Features



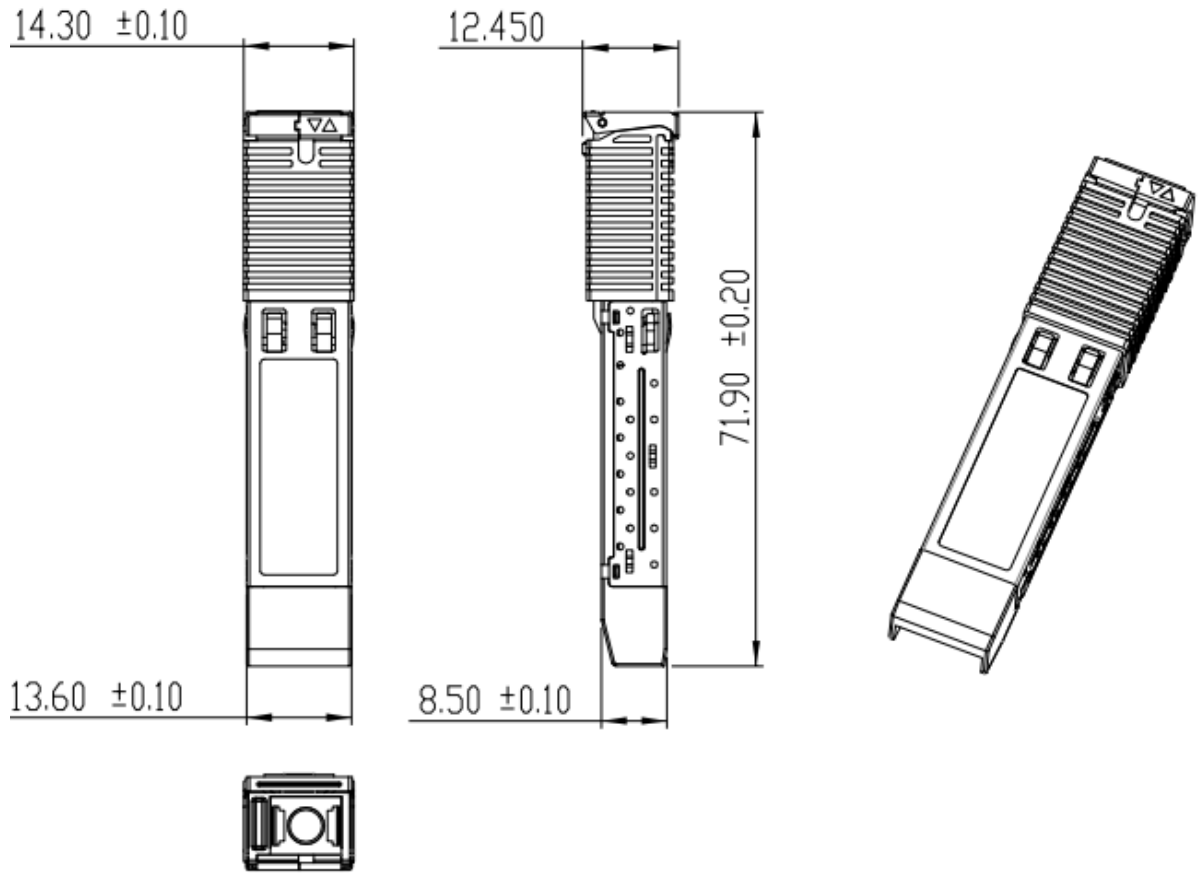
Operation

- (1) If Dying_GASP Reference Voltage Hysteris can over 26mV, 80mV or 130mV,
The GPON STICK send PLOAMu message with "DYING_GASP Status" to OLT
- (2) To activate this Dying_Gasp Features, System Operator or OLT system can configure Dying_Gasp Registers with 26mV, 80mV or 130mV
- (3) Default Dying_Gasp Register is 80mV

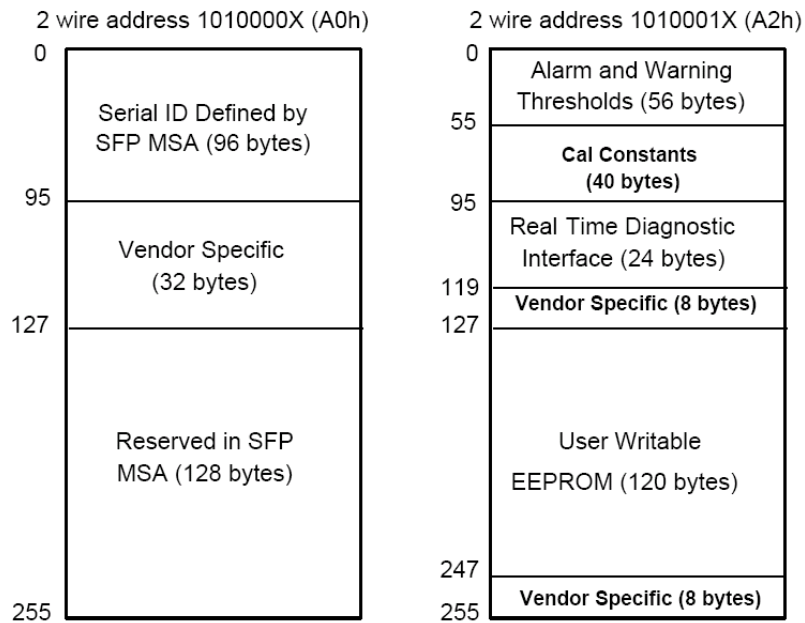
Typical Interface Circuit



Mechanical Diagram



EEPROM Memory Map



A0 EEPROM definition table (the registers in red color are writable)

TYPE	OFFSET		# Bytes	NAME
	HEX	DEC		
BASE	0x00	0	1	Identifier
	0x01	1	1	Ext. Identifier
	0x02	2	1	Connector
	0x03	3月10日	8	Transceiver
	0x0b	11	1	Encoding
	0x0c	12	1	Bit Rate, Nominal
	0x0d	13	1	Rate Identifier
	0x0e	14	1	Length (SMF, km)
	0x0f	15	1	Length (SMF, 100m)
	0x10	16	1	Length (50um)
	0x11	17	1	Length (62.5um)
	0x12	18	1	Length (copper)
	0x13	19	1	Length (OM3)
	0x14	20 - 35	16	Vendor name
	0x24	36	1	Transceiver
	0x25	37 - 39	3	Vendor OUI
	0x28	40 - 55	16	Vendor PN
	0x38	56 - 59	4	Vendor rev
	0x3c	60 - 61	2	Wavelength
	0x3e	62	1	Reserved
0x3f	63	1	CC_BASE	
EXTENDED	0x40	64	1	Options
	0x41	65	1	Options
	0x42	66	1	BR, max
	0x43	67	1	BR, min
	0x44	68 - 83	16	Vendor SN
	0x54	84 - 85	2	Date (Year)
	0x56	86 - 87	2	Date (Month)
	0x58	88 - 89	2	Date (Day)
	0x5a	90 - 91	2	Lot Code
	0x5c	92	3	Diagnostic Monitoring Type
	0x5d	93		Enhanced Options
	0x5e	94		SFF8472 Compliance
	0x5f	95		CC_EXT
VENDOR	0x60	96 - 127		Vendor Specific
	0x80	128 - 255		Reserved